PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2001-274034

(43)Date of publication of application : 05.10.2001

(51)Int.Cl. H01G 2/06
H01G 4/33
H01G 4/10
H01G 4/12
H01L 23/12
H01L 25/00
H05K 9/00

(21)Application number : 2000-276514

(22)Date of filing : 12.09.2000

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(30)Priority

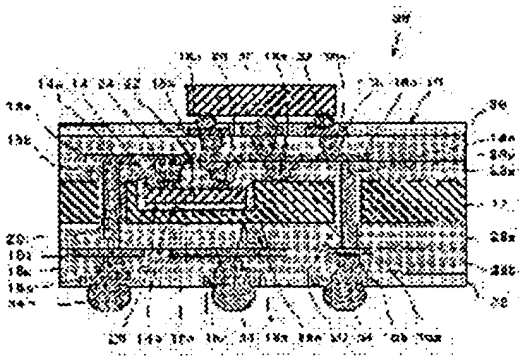
Priority number : 2000011767 Priority date : 20.01.2000 Priority country : JP

(54) ELECTRONIC PARTS PACKAGE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide an electronic parts package in which electronic parts can be packed at a high density and, at the same time, which can shield the parts from electromagnetic noise.

SOLUTION: This electronic parts package 10 has a recessed section 14 formed into a core material 12, a semiconductor chip 22 buried in the section 14, insulating layers 28a and 28b formed on the surface of the material 12 on the opening side of the recessed section 14 so as to cover the section 14. This package also has wiring layers 16a and 16b formed on the



surfaces of the insulating layers 28a and 28b and via holes 18a and 18b which are formed through the insulating layers 28a and 28b and electrically connect the wiring layers 16a and 16b to electrode terminals 24 formed on the surface of the semiconductor chip 22 on the opening side of the recessed section 14. The internal wall surface 14a and bottom face 14b of the recessed section 14 are composed of a conductive metal.

LEGAL STATUS

[Date of request for examination]	15.10.2002
[Date of sending the examiner's decision of rejection]	
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	
[Date of registration]	
[Number of appeal against examiner's decision of rejection]	
[Date of requesting appeal against examiner's decision of rejection]	
[Date of extinction of right]	

* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The crevice formed in core material, the electronic parts embedded in this crevice, and the insulating layer formed so that this crevice might be covered on the front face of said core material by the side of opening of said crevice, In the electronic-parts package possessing the beer which connects electrically the wiring layer formed in the front face of this insulating layer, and the electrode which was formed in said insulating layer and formed in the front face by the side of this wiring layer and crevice opening of said electronic parts The electronic-parts package whose internal surface and base of said crevice are characterized by being a conductive metal.
[Claim 2] The electronic-parts package according to claim 1 said whose core material is characterized by consisting of a conductive metal.
[Claim 3] The electronic-parts package according to claim 1 characterized by being covered with the plating coat with which said core material consists of an insulating material, and the internal surface and base of said crevice consist of a conductive metal.
[Claim 4] The electronic-parts package according to claim 1, 2, or 3 said whose electronic parts are characterized by being a semiconductor chip.
[Claim 5] Said electronic parts are the capacitor by which the electrode was formed in front flesh-side both sides, an inductor, or resistance. A rear-face side is joined to the base of said crevice through the conductive layer formed using the conductive adhesion paste or the conductive adhesion sheet. The electronic-parts package according to claim 1, 2, or 3 characterized by connecting electrically the electrode by the side of a rear face to said wiring layer through the conductive metal of the internal surface of this conductive layer and said crevice, and a base.
[Claim 6] The electronic-parts package according to claim 5 characterized by providing the metal layer which said capacitor becomes from the platinum formed in one field of the sheet metal which consists of p-type silicon, and this sheet metal, the dielectric layer formed in the field of another side of said sheet metal, and the electrode formed on this dielectric layer.
[Claim 7] The electronic-parts package according to claim 5 characterized by providing the metal layer which said capacitor becomes from the titanium or lead formed in one field of the sheet metal which consists of n mold silicon, and this sheet metal, the dielectric layer formed in the field of another side of said sheet metal, and the electrode formed on this dielectric layer.
[Claim 8] The electronic-parts package according to claim 5 characterized by said capacitor being a capacitor by which the oxide skin was formed by the anodization method on the surface of the metallic foil, and the electrode was formed on this oxide skin.
[Claim 9] The electronic-parts package according to claim 5 characterized by said capacitor being a capacitor by which the dielectric layer was formed in the front face of a titanium metallic foil the hydrothermal crystallization method, and the electrode was formed on this dielectric layer.
[Claim 10] The electronic-parts package according to claim 1, 2, or 3 said whose electronic parts are characterized by being a capacitor.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the electronic-parts package which embedded and carried electronic parts, such as a semiconductor chip, a capacitor, and an inductor, in core material at the detail further about an electronic-parts package.
[0002]
[Description of the Prior Art] Conventionally, what was indicated by patent No. (JP,9-321408,A) 2842378 is well-known as what embeds electronic parts (a semiconductor chip, a capacitor, resistance, and inductor) in the crevice formed in core material, carries out the laminating of an insulating layer and the wiring layer so that a crevice may be covered after that to front flesh-side both sides of the core material by the side of opening of a crevice, and forms an electronic-parts package. By adopting this structure, the densification of the mounting of the electronic parts to an electronic-parts package can be carried out.
[0003]
[Problem(s) to be Solved by the Invention] by the way, the electromagnetism which the frequency of the electrical signal which flows in recent years to the clock frequency of the electronic parts mounted in an electronic-parts package or electronic parts high-frequency-izes, and is generated on an electronic-parts package in connection with it -- the noise has been increasing. For this reason, an electronic-parts package of the structure which can shield electronic parts from a noise is desired so that malfunction by the noise etc. can be prevented. However, since electronic parts are only embedded with the structure of patent No. 2842378 where it explained in the conventional example at the printed circuit board as core material which consists of a resin ingredient, the embedded electronic parts are not surrounded with a conductor, but there is nothing that is called the electromagnetic shielding structure from a noise. Therefore, the technical problem that the electronic parts mounted in the circuit board gather a noise, and malfunction, and it superimposes on the electrical signal with which the noise which electronic parts gathered flows to electronic parts occurs.
[0004] therefore, do this invention that the above-mentioned technical problem should be solved -- electromagnetism [as opposed to / while the place made into the purpose can mount electronic parts in high density / electronic parts] -- it is in offering the electronic-parts package which also has a shielding effect from a noise.
[0005]
[Means for Solving the Problem] The crevice formed in core material in order that this invention might solve the above-mentioned technical problem, and the electronic parts embedded in this crevice, The insulating layer formed so that this crevice might be covered on the front face of said core material by the side of opening of said crevice, In the electronic-parts package possessing the beer which connects electrically the wiring layer formed in the front face of this insulating layer, and the electrode which was formed in said insulating layer and formed in the front face by the side of this wiring layer and crevice opening of said electronic parts The internal surface and base of said crevice are characterized by being

a conductive metal. Moreover, said core material can specifically adopt the configuration which consists of a conductive metal. Moreover, the configuration covered with the plating coat with which said core material consists of an insulating material, and the internal surface and base of said crevice consist of a conductive metal is also employable. While according to these configurations it is high-density and being able to mount electronic parts, since the electronic parts embedded in the crevice are covered with a conductive metal except for a crevice opening part, electromagnetic shielding of them is carried out to a noise, and they are effective in the effect of the noise to the electronic parts in a crevice being mitigated.

[0006] Moreover, said electronic parts can also adopt the configuration which is a semiconductor chip. Moreover, said electronic parts are the capacitor by which the electrode was formed in front flesh-side both sides, an inductor, or resistance, and the electrode by the side of a rear face is able to be joined to the base of said crevice through the conductive layer in which the rear-face side was formed using the conductive adhesion paste or the conductive adhesion sheet, and to consider as the configuration electrically connected to said wiring layer through the conductive metal of the internal surface of this conductive layer and said crevice, and a base.

[0007] The capacitor possessing the sheet metal which becomes said capacitor from p-type silicon, the metal layer which consists of platinum formed in one field of this sheet metal, the dielectric layer formed in the field of another side of said sheet metal, and the electrode formed on this dielectric layer can be used. Or the capacitor possessing the sheet metal which becomes said capacitor from n mold silicon, the metal layer which consists of the titanium or lead formed in one field of this sheet metal, the dielectric layer formed in the field of another side of said sheet metal, and the electrode formed on this dielectric layer can be used.

[0008] Moreover, the capacitor by which the oxide skin was formed in said capacitor by the anodization method on the surface of the metallic foil, and the electrode was formed on this oxide skin can be used. Moreover, the capacitor by which the dielectric layer was formed in the front face of a titanium metallic foil the hydrothermal crystallization method, and the electrode was formed on this dielectric layer at said capacitor can be used. Or a capacitor may be used for said electronic parts.

[0009]

[Embodiment of the Invention] Hereafter, the gestalt of suitable implementation of the electronic-parts package concerning this invention is explained to a detail based on an accompanying drawing.

(Gestalt of the 1st operation) The structure of the electronic-parts package 10 is explained. The crevice 14 is formed in the core material 12. With the gestalt of this operation, the core material 12 forms conductive metals, such as copper, in tabular. And using devices, such as a router, the front face of the core material 12 is deleted and formed, and this crevice 14 forms it by etching. Moreover, the flat-surface configuration of a crevice 14 is set as the configuration where electronic parts can be held, in consideration of the magnitude of the electronic parts embedded in a crevice 14. Since the flat-surface configuration of the electronic parts carried in the electronic-parts package 10 is usually a square, as for the flat-surface configuration of a crevice 14, it is common to this to consider as 4 in all square shapes, and it is also possible for it not to be limited to this and to consider as polygons other than a round shape or a square.

[0010] Moreover, although the depth of a crevice 14 has the desirable depth of extent in which electronic parts are completely held and electronic parts do not project from a crevice 14 in order to heighten the shielding effect to a noise, it is not limited to this. Moreover, the through tube 20 for letting the beer 18 which connects electrically wiring layer 16 comrades arranged at the front face and rear face of the core material 12 besides a crevice 14 pass is formed in the core material 12 by the same means as a crevice 14.

[0011] And in the crevice 14, the semiconductor chip 22 is embedded as an example of electronic parts. The embedded structure of a semiconductor chip 22 turns to the opening side of a crevice 14 the field (henceforth an electrode terminal forming face) in which the electrode (it is also called an electrode terminal) 24 was formed in the semiconductor chip 22, it uses adhesives 26 for the base of a crevice 14, pastes up the field by the side of reverse (tooth back) on it, and holds and fixes it in a crevice 14.

[0012] And in this sequence, on the front face of the core material 12 by the side of opening of a crevice 14, a laminating is carried out to a multilayer and the electric insulating layer (only henceforth an insulating layer) 28 and the wiring layer 16 are formed in front flesh-side both sides of the core material 12 so that a crevice 14 may be covered. And each wiring layer 16 is electrically connected by the beer 18 which penetrates an insulating layer 28 and the core material 12. Also in three or more layers, a view is the same, although the two-layer [every] laminating of an insulating layer 28 and the wiring layer 16 is carried out to front flesh-side both sides of the core material 12 as an example, respectively and they are formed in them with the gestalt of this operation. An insulating layer 28 consists of 1st insulating-layer 28a and 2nd insulating-layer 28b of the upper layer. Moreover, a wiring layer 16 consists of 1st wiring layer 16a formed in the front face of 1st insulating-layer 28a, and 2nd wiring layer 16b formed in the front face of 2nd insulating-layer 28b. Moreover, beer 18 penetrates the insulating layer 28 arranged at one field side of the core material 12. 1st beer 18a which connects the electrode terminal 24 of a semiconductor chip 22 with wiring layer 16 comrades arranged at the field side of one of these, a wiring layer 16 and the core material 12, or a wiring layer 16 electrically, It consists of 2nd beer 18b which connects electrically wiring layer 16 comrades which penetrated the through tube 20 of the core material 12, and were formed in the front flesh side of the core material 12.

[0013] And the enveloping layer 36 by the solder resist is formed in the front face of 2nd insulating-layer 28b or 2nd wiring layer 16b so that only the predetermined part of 2nd wiring layer 16b used as the land in which the bump 32 of a semiconductor chip 30 and the external connection terminal 34 of the electronic-parts package 10 which are carried in the electronic-parts package 10 are attached may be exposed. The above is the configuration of the electronic-parts package 10. In addition, where the external connection terminal 34 is attached in the land of 2nd wiring layer 16b, it may consider as the electronic-parts package 10. Moreover, the two or more number of the crevices 14 formed in the core material 12 is formed, it is good also as a configuration which embeds two or more electronic parts into the core material 12, it is possible not only one front face of the core material 12 but to consider as the structure which forms a crevice 14 in both sides and embeds electronic parts, and further densification can be attained.

[0014] And other semiconductor chips 30 are carried in the front face (top face in drawing 1) of this electronic-parts package 10 through a bump 32, and the external connection terminals 34, such as a solder ball, are connected to the rear face (inferior surface of tongue in drawing 1) of the electronic-parts package 10, and it becomes a semiconductor device 38. In such the electronic-parts package 10 and a semiconductor device 38, since internal-surface 14a and base 14b of a crevice 14 are a conductive metal, internal-surface 14a and base 14b of a crevice 14 of the core material 12 become an electromagnetic shielding wall, and the noise generated in electronic parts and the wiring layer of the others carried in the electronic-parts package 10 can mitigate extent which has a direct bad influence on the semiconductor chip 22 in a crevice 14. Furthermore, although it is thick as compared with a wiring layer 16 and the core material 12 used as the potential stabilized since electric resistance was low is usually used as a grand layer, it also has effectiveness very much in noise mitigation that the semiconductor chip 22 embedded in the crevice 14 of the core material 12 with the conductive metal used as the potential stabilized in this way is surrounded.

[0015] Furthermore, the life of the semiconductor chip 22 with which the heat generated with a semiconductor chip 22 escapes efficiently to the core material 12, is effective in a semiconductor chip 22 being cooled efficiently with the semiconductor chip, and was embedded since the tooth back had pasted up the semiconductor chip 22 in a crevice 14 on the core material 12 is prolonged, and it is thought that the stability of the electronic-parts package 10 or a semiconductor device 38 increases as a result. Furthermore, since it holds in the crevice 14 formed in the metal core material 12 which has rigidity compared with resin material even if a semiconductor chip 22 is very thin, even if external force is added, the effectiveness of being hard to produce a crack is in a semiconductor chip 22.

[0016] Next, the manufacture approach of the electronic-parts package 10 is explained using drawing 4 - drawing 13 . First, a copper substrate is prepared as core material 12 as an example of a conductive metal (refer to drawing 4). And a crevice 14 is formed in the front face of the core material 12 by

etching or router processing (refer to drawing 5). Next, a through tube 20 is formed in the location which makes 2nd beer 18b of the core material 12 penetrate (refer to drawing 6). Next, the semiconductor chip 22 as electronic parts is pasted up in the crevice 14 of the core material 12 (refer to drawing 7).

[0017] Next, while forming 1st insulating-layer 28a in front flesh-side both sides of the core material 12 so that a crevice 14 may be covered, it is filled up with the resin ingredients (PPE resin etc.) which form 1st insulating-layer 28a in the through tube 20 of the core material 12, or a crevice 14 (refer to drawing 8). Next, a laser beam is irradiated and the 1st beer hole 52 and the 2nd beer hole 54 are formed in 1st insulating-layer 28a. The 1st beer hole 52 is formed as an exposure hole which the electrode terminal 24 of a semiconductor chip 22 and the front face of the core material 12 expose to a base. Moreover, the 2nd beer hole 54 is formed in the resin with which the through tube 20 of the core material 12 was filled up, and the configuration which penetrates 1st insulating-layer 28a formed in front flesh-side both sides of the core material 12. In case the 2nd beer hole 54 is formed, it is made not exposed [the internal surface of a through tube 20] here (refer to drawing 9). In addition, as the technique of forming a beer hole in an insulating layer, it replaces with a laser beam exposure and the technique which etches chemically and is formed is also considered.

[0018] Next, while performing non-electrolytic copper plating and electrolytic copper plating and forming a metal plating coat in the front face of 1st insulating-layer 28a, the inside of the 1st beer hole 52 and the 2nd beer hole 54 is filled up with a conductor. And the metal plating coat of the front face of 1st insulating-layer 28a is etched according to a predetermined pattern, and 1st wiring layer 16a is formed. The wiring layer of a predetermined pattern can be formed by applying a photosensitive resist to the front face of a metal plating coat, exposing and developing a photosensitive resist, forming a resist pattern, and removing the exposed part of the metal plating coat of the part which is not covered with a resist pattern (refer to drawing 10). Here, it fills up with a conductor in the 1st beer hole 52, and is set to 1st beer 18a, and it fills up with a conductor in the 2nd beer hole 54, and is set to 2nd beer 18b.

[0019] Next, 2nd insulating-layer 28b is formed so that the front face of 1st insulating-layer 28a of front flesh-side both sides of the core material 12 and 1st wiring layer 16a may be covered. And a laser beam is irradiated and the 1st beer hole 52 is formed in 2nd insulating-layer 28b (refer to drawing 11). This 1st beer hole 52 is formed in a base as an exposure hole which the predetermined part of 1st wiring layer 16a exposes. Next, while performing non-electrolytic copper plating and electrolytic copper plating and forming a metal plating coat in the front face of 2nd insulating-layer 28b, the inside of the 1st beer hole 52 is filled up with a conductor. And the metal plating coat of the front face of 2nd insulating-layer 28b is etched like the case of 1st wiring layer 28a according to a predetermined pattern, and 2nd wiring layer 16b is formed (refer to drawing 12). 1st beer 18a is formed by filling up the inside of the 1st beer hole 52 with a conductor.

[0020] The enveloping layer 36 by the solder resist is formed so that only the predetermined part of 2nd wiring layer 16b used as the land by which the bump 32 of a semiconductor chip 30 and the external connection terminal 34 of the electronic-parts package 10 which are carried in the electronic-parts package 10 are finally attached in the front face of 2nd insulating-layer 28b and 2nd wiring layer 16b may be exposed (refer to drawing 13). The above is the manufacture approach of the electronic-parts package 10.

[0021] (Gestalt of the 2nd operation) The structure of the electronic-parts package 40 is explained. First, when the outline is explained about difference with the gestalt of the 1st operation, the core material 12 of the gestalt of this operation is in the point which consists of boards formed with the ingredient (insulating material) which has electric insulation, such as a glass epoxy group plate and BT (bismaleimide triazine) substrate. For this reason, in order to shield the electronic parts embedded in the crevice 14 of the core material 12, in case a wiring layer 42 is formed in the front face of the core material 12, internal-surface 14a and base 14b of a crevice 14 are also considered as the configuration which carries out electromagnetic shielding of the electronic parts which cover with the metal plating coat 44 which has the conductivity which forms this wiring layer 42, and are held in a crevice 14 with this metal plating coat 44.

[0022] Since the structure of the insulating layer 28, the wiring layer 16, and enveloping layer 36 which carry out a laminating to the core material 12 only by the structure of the part about the core material 12 being different is the same as the gestalt of the 1st operation, the sign same about the same configuration is attached, explanation is omitted, and only a different configuration is explained. The crevice 14 is formed in the core material 12. With the gestalt of this operation, the core material 12 forms the above insulating materials in tabular. The wiring layer 42 is formed in the front face and rear face of the core material 12. Moreover, internal-surface 14a and base 14b of a crevice 14 are covered with the metal plating coat 44 which has the conductivity which forms this wiring layer 42.
[0023] The 2nd beer 18 which penetrates the core material 12 connects electrically 1st wiring layer 16a formed in the front face of the wiring layer 42 formed in the front face of wiring layer 42 comrades formed in the front face of the core material 12, or the core material 12, and an insulating layer 28. In addition, although wiring layer 42 comrades formed in the front face of the core material 12 among the 2nd beer 18 are connected, and structure comes to fill up resin 48 after forming the metal plating coat 46 in the inner skin of the through tube 20 formed in the core material 12 as an example, other structures are sufficient as it. Moreover, the metal plating coat 44 formed in internal-surface 14a and base 14b of a crevice 14 is electrically connected with the bump for glands of a semiconductor chip 30 and/or the external connection terminal 34 which are carried in the electronic-parts package 40 by 1st beer 18a and/or 2nd beer 18b. With the gestalt of this operation, the metal plating coat 44 in a crevice 14 While connecting with the bump for glands of a semiconductor chip 30 through the wiring layer 42 and 1st beer 18a which were formed in the front face of the core material 12, 1st wiring layer 16a, and 2nd wiring layer 16b 2nd beer 18b which penetrates 1st insulating-layer 28a and the core material 12, and reaches base 14b of a crevice 14 connects also with the external connection terminal 34 electrically.
[0024] Even if the core material 12 is formed by the insulating material, thus, internal-surface 14a and base 14b of the crevice 14 in which the semiconductor chip 22 embedded into the core material 12 is held Since it is covered with the metal plating coat 44 which has conductivity and has predetermined potential (for example, ground potential), It becomes possible to reduce that electromagnetic shielding of the semiconductor chip 22 is carried out with the metal plating coat 44, and a noise jumps into the direct semiconductor chip 22 like the gestalt of the 1st operation.
[0025] (Gestalt of the 3rd operation) In the gestalt of each operation mentioned above, although the semiconductor chip 22 was mentioned as the example and has been explained as electronic parts held and embedded in the crevice 14 of the core material 12, besides semiconductor chip 22, other electronic parts, such as resistance and a capacitor, can be held in a crevice 14, and it can embed into the core material 12. And the electronic parts 50, such as a capacitor, resistance, and an inductor, can be constituted from forming coat 50b of a dielectric material or electrical resistance materials in the front face of silicon substrate 50a used as a lower electrode, as shown in drawing 3 , and forming conductive film 50c used as an up electrode in the front face of this coat 50b.
[0026] By using the adhesives (conductive layer) which have the conductivity of a conductive paste or a conductive adhesion sheet in the electronic parts 50 of this structure for the adhesives 26 at the time of pasting up silicon substrate 50a which is a lower electrode in a crevice 14 Since it becomes possible to connect lower electrode 50a of electronic parts 50 with the metal plating coat 44 electrically formed in base 14b of a crevice 14, by using the 2nd electronic-parts package 40 of the structure of the gestalt of operation It becomes possible about base 14b and internal-surface 14a of a crevice 14 to connect the wrap metal plating coat 44 with the semiconductor chip 30, other electronic parts, and the external connection terminal 34 which used it as a wiring layer and were carried in the electronic-parts package 10 electrically. In addition, in drawing 3 , although explained using the 2nd electronic-parts package 40 of the gestalt of operation as an example, the electronic parts 50, such as a capacitor, resistance, and an inductor, as well as the 1st electronic-parts package 10 of the gestalt of operation can be carried.
[0027] An example of a capacitor 50 is shown in drawing 14 . When using a silicon substrate for lower electrode 50a, it is suitable in using the sheet metal which consists of a p mold or n mold silicon (it explains as sheet metal 50a below). This sheet metal 50a carries out polishing of the silicon wafer, thins in thickness of about 30-50 micrometers, and is cut and formed in necessary size. By carrying out

polishing of the wafer, a front face turns into a mirror plane and becomes what has high display flatness.

[0028] 50d of metal layers is formed on one field of this sheet metal 50a. 50d of metal layers is used as the layer of platinum when sheet metal 50a is p-type silicon, and when sheet metal 50a is n mold silicon, let them be the layer of titanium or lead. 50d of these metal layers can be formed in one field of sheet metal 50a by sputtering or vacuum evaporationo. Although especially the thickness of 50d of metal layers is not limited, it can be made into a several micrometers - dozens of micrometers thing.
[0029] With n mold silicon, between sheet metal 50a and 50d of metal layers, 50d of metal layers serves as ohmic contact so that clearly from the difference of a work function, when it is titanium or lead, and sheet metal when sheet metal 50a is [50d of metal layers] platinum in p-type silicon 50a conducts any current of a direction. When the combination of sheet metal 50a and 50d of metal layers is except the above, it becomes shot key connection, and rectification arises, and only the current of a certain one direction flows.
[0030] Coat 50b which consists of a dielectric material by sputtering etc. is formed in the field of another side of sheet metal 50a. The capacitor of high capacity is obtained, so that the thickness of coat 50b is thin. Since sheet metal 50a can carry out polishing of the wafer and can obtain it as mentioned above although the display flatness of sheet metal 50a is important in order to obtain thin coat 50b, it is large, therefore the formation of thin coat 50b without a pinhole of the display flatness is attained.
[0031] If dielectric materials, such as tantalum oxide (Ta 2O5), strontium titanate (SrTiO3), barium titanate (BaTiO3), titanic-acid lead zirconate (PbZrx Ti1-xO3), or strontium titanate barium (Bax Sr1-xTiO3), are used for coat 50b, it is suitable for it.
[0032] Conductive film 50c which is an up electrode is formed on coat 50b. Conductive film 50c is good to form a chromium layer (not shown) by sputtering first on coat 50b, and to form a copper layer by sputtering etc. on this chromium layer in order to raise adhesion with coat 50b. It is suitable, if many capacitors 50 of the above-mentioned configuration are made on a silicon wafer, this is cut and it is made to separate into the capacitor 50 of the piece of an individual. 50d of metal layers is turned to the base side of a crevice 14, and the above-mentioned capacitor 50 is fixed on the metal plating coat 44 with electroconductive glue 26.
[0033] Drawing 15 shows the gestalt of the operation of further others of a capacitor 50. 13 is bulb metallic foils, such as aluminum, titanium, and a tantalum. An oxide skin 15 is formed in a front face by the anodization method (anodic oxidation) well-known to this bulb metallic foil 13. The bulb metallic foil 13 can use a 5 micrometers - about 30 micrometers thin thick thing, and can form the about 0.3-micrometer very thin oxide skin 15 in the front face of this bulb metallic foil 13. The thing wound in the shape of a roll or the sheet-like thing which has a large area can be used for the bulb metallic foil 13, and it can perform anode plate chemical conversion efficiently.
[0034] On the oxide skin 15 of both sides of the bulb metallic foil 13, a copper layer is formed by sputtering or vacuum evaporationo, and electrode layers 17 and 17 are formed. It judges in the magnitude of a request of this bulb metallic foil 13, and forms in a capacitor 50. Although an oxide skin 15 is hard and it is weak, since the flexible bulb metallic foil 13 exists in the heart, as a whole, brittleness is reduced and it is easy to deal with it. In addition, although the oxide skin 15 and the electrode layer 17 were formed in both sides of the bulb metallic foil 13, you may make it form an oxide skin 15 and an electrode layer 17 only in one side of the bulb metallic foil 13 above.
[0035] Moreover, although the oxide skin 15 as a dielectric layer was formed by anode plate chemical conversion on the bulb metallic foil 13 with the gestalt of the above-mentioned implementation, the crystal film of the titanic-acid lead zirconate which is a ferroelectric, strontium titanate, barium titanate, and strontium titanate barium is formed on a titanium metallic foil with a hydrothermal crystallization method, and it is good also as a dielectric layer (not shown). In order to make the titanic-acid lead zirconate (PZT) crystal film generate with a hydrothermal crystallization method, a titanium metallic foil is immersed in the strong-base solution in which the lead compound, the zircon compound, and the titanium compound were dissolved, put in into the autoclave set as 200 degrees C or less and 2 - 3atm (1atm=1.01325bar) extent, a hydrothermal synthesis reaction is made to cause, and it is made to make

the PZT crystal film generate. Other dielectric layers can be formed with a necessary hydrothermal crystallization method. Thus, the titanium metallic foil in which the dielectric layer was formed can be judged, and it can be made a capacitor.

[0036] Drawing 16 shows the gestalt of the operation of further others of a capacitor 50. This capacitor 50 is a multi-electrode capacitor which the electrode was multipolarized and has been arranged in the shape of a matrix. This multi-electrode capacitor has the advantage which can reduce the parasitism inductance which the capacitor itself has and can reduce the inductance of the whole electronic-parts package incorporating this. This capacitor 50 as well as the above is incorporable in a crevice 14. In addition, it cannot be overemphasized that connection is electrically taken through beer to each multipolar electrode.

[0037] Next, the manufacture approach of the electronic-parts package 40 is explained using drawing 17 - drawing 26 . In addition, the sign same about the same processing as the 1st electronic-parts package 10 of the gestalt of operation is attached, and explanation is omitted. First, double-sided copper-clad ****** is prepared as core material 12 as the resin substrate with which conductor-layer 12b was formed in both sides of tabular resin base material 12a, and an example (refer to drawing 17). And the crevice 14 formed in the front face of the core material 12 by the resin in which base 14b and internal-surface 14a form resin base material 12a by etching or router processing, and the through tube 20 which the resin which forms resin base material 12a exposes to an inside are formed (refer to drawing 18). Next, while forming an electrolysis plating coat in base 14b of the front face of the core material 12, and a crevice 14, and internal-surface 14a by the same technique as drawing 10 , the inside of a through tube 20 is filled up with a conductor (plating). And pattern NINGU of the electrolysis plating coat of the front face of the core material 12 is carried out, and a wiring layer 42 is formed in front flesh-side both sides of the core material 12 (refer to drawing 19). It leaves the electrolysis plating coat of base 14b of a crevice 14, and internal-surface 14a, without etching, and it is made into the condition of having connected with some wiring layers 42. 2nd beer 18b is formed by filling up the inside of a through tube 20 with a conductor (plating).

[0038] Next, electronic parts 50 are carried in a crevice 14. Although electronic parts 50 are the capacitors by which the electrode (a lower electrode is silicon substrate 50a, and an up electrode is conductive film 50c) was formed in front flesh-side both sides as an example, the same is said of the case of other electronic parts (refer to drawing 20). It is made to flow through the lower electrode of electronic parts 50 with the electrolysis plating coat 44 formed in adhesives at base 14b of a crevice 14 using the conductive ingredient. Next, 1st insulating-layer 28a is formed in front flesh-side both sides of the core material 12 so that a crevice 14 and electronic parts 50 may be covered (R> drawing 21 1 reference). Next, a laser beam is irradiated and the 1st beer hole 52 which up electrode 50c of the front face of a wiring layer 42 or electronic parts 50 exposes on a base is formed in 1st insulating-layer 28a. Furthermore, a laser beam is irradiated from the rear-face side of the core material 12, and the 2nd beer hole 54 which exposes on a base the metal plating coat 44 which penetrated 1st insulating-layer 28a and the core material 12, and was formed in base 14b of a crevice 14 is formed (refer to drawing 22).

[0039] Next, like drawing 10 , non-electrolytic copper plating and electrolytic copper plating are performed, and a metal plating coat is formed in the front face of 1st insulating-layer 28a. Moreover, the inside of the 1st beer hole 52 and the 2nd beer hole 54 is filled up with a conductor, and 1st beer 18a and 2nd beer 18b are formed. And the metal plating coat of the front face of 1st insulating-layer 28a is etched according to a predetermined pattern, and 1st wiring layer 16a is formed (refer to drawing 23). Next, 2nd insulating-layer 28b is formed so that the front face of 1st insulating-layer 28a of front flesh-side both sides of the core material 12 and 1st wiring layer 16a may be covered (refer to drawing 24). Next, while irradiating a laser beam and forming the 1st beer hole 52 in 2nd insulating-layer 28b, 2nd wiring layer 16b and 1st beer 18a are formed like drawing 12 (refer to drawing 25). And finally the enveloping layer 36 by the solder resist is formed in the front face of 2nd insulating-layer 28b and 2nd wiring layer 16b like drawing 13 (refer to drawing 26). The above is the manufacture approach of the electronic-parts package 40.

[0040]

[Effect of the Invention] While according to the electronic-parts package concerning this invention it is high-density and being able to mount electronic parts, since the electronic parts embedded in the crevice are covered by conductive metal material except for a crevice opening part, electromagnetic shielding of them is carried out to a noise, and they are effective in the effect of the noise to the electronic parts in a crevice being mitigated.

[Translation done.]

* NOTICES *

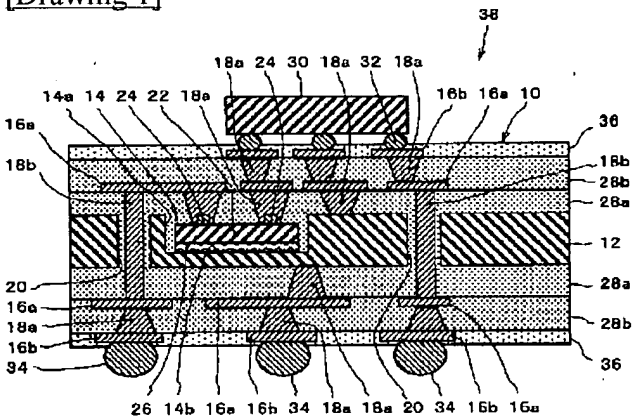
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

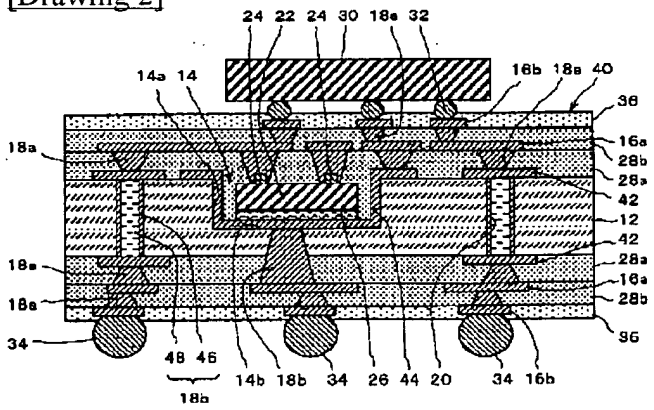
[Drawing 4]

[Drawing 5]

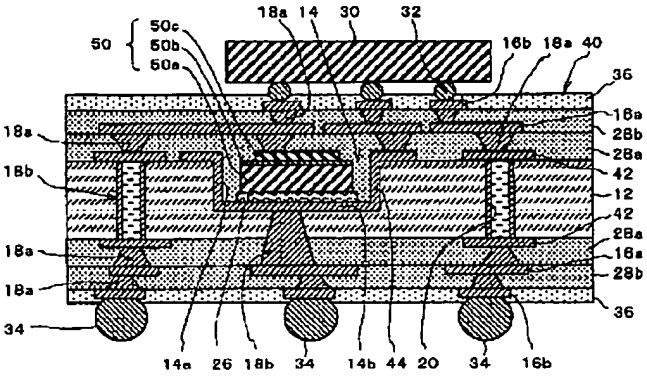
[Drawing 1]



[Drawing 2]

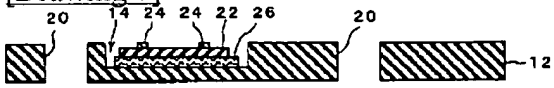


[Drawing 3]

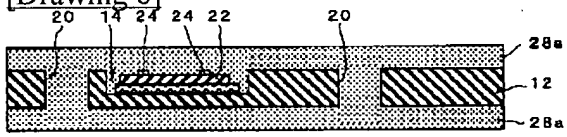


[Drawing 6]

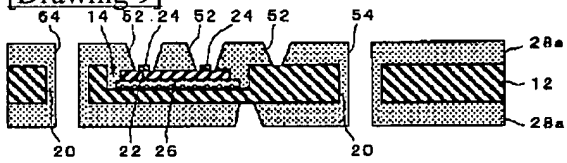
[Drawing 7]



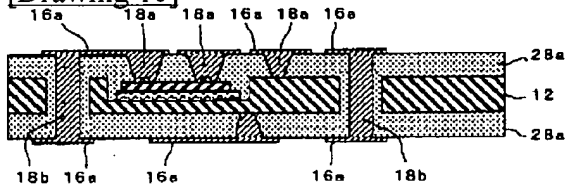
[Drawing 8]



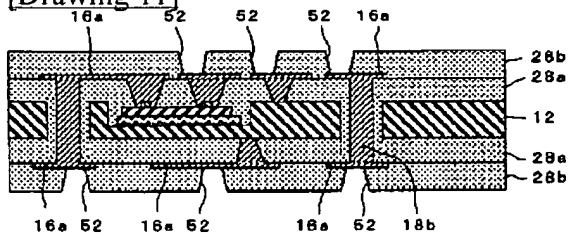
[Drawing 9]



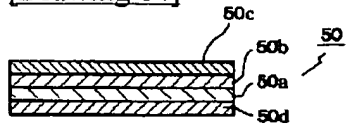
[Drawing 10]



[Drawing 11]



[Drawing 14]



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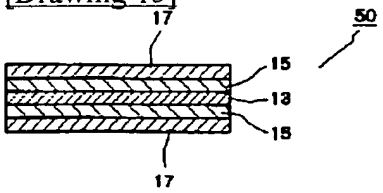
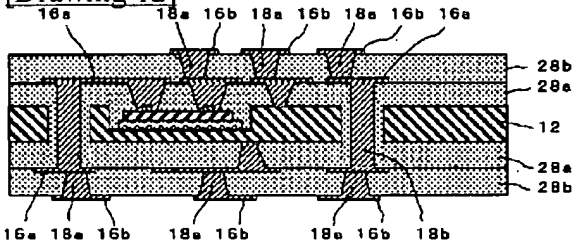
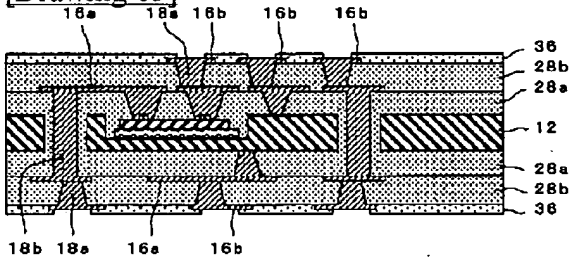


[Drawing 17]

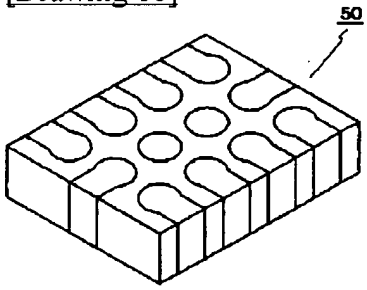
[Drawing 12]



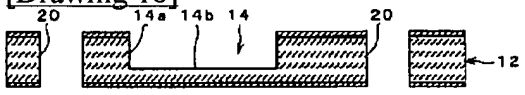
[Drawing 13]



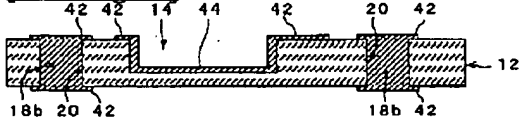
[Drawing 16]



[Drawing 18]



[Drawing 19]



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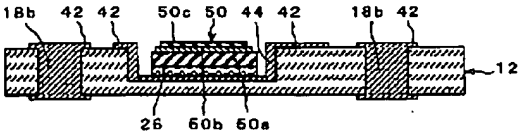
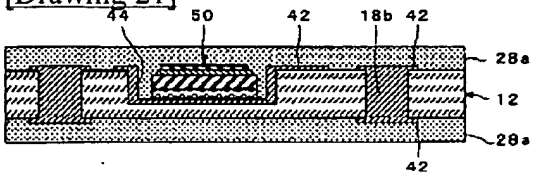


[Drawing 21]



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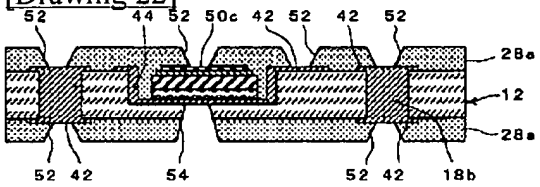
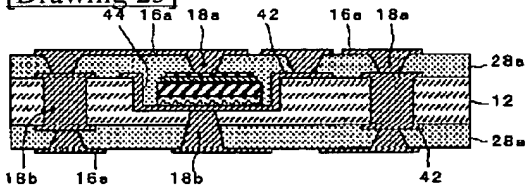
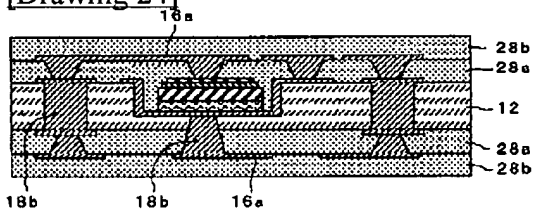


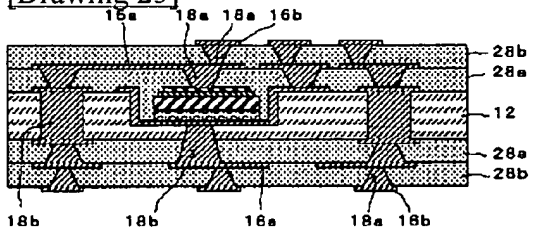
[Drawing 23]



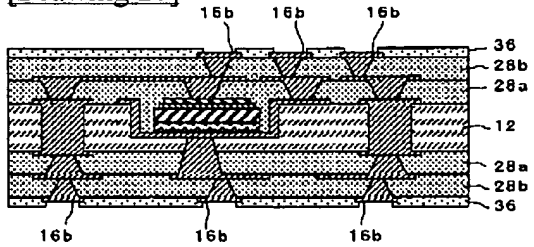
[Drawing 24]



[Drawing 25]



[Drawing 26]



[Translation done.]